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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

| Docket Number (Optional) |
|---|
| JRL-550-477 |

| Application Number | Filed |
|---|---|
| 10/714,178 | November 17, 2003 |
| **First Named Inventor** | |
| ORION | |
| **Art Unit** | **Examiner** |
| 2436 | Daniel L. HOANG. |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

June 30, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.



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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

ORION et al.

Appl. No. 10/714,178

Filed: November 17, 2003


Atty. Ref.: 550-477; Confirmation No. 9349

TC/A.U. 2436

Examiner: Daniel L. HOANG.

For: DIAGNOSTIC DATA CAPTURE CONTROL FOR MULTI-DOMAIN PROCESSORS

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June 30, 2010

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## THIRD PRE-APPEAL BRIEF REQUEST FOR REVIEW

This is the third pre-appeal where Gonzales is used as the primary reference combined with some secondary reference to reject claims 1-7 and 10-17. This third time, the new secondary reference is Moroney. This rejection is respectfully traversed.

**Clear Error #1: Gonzales and Moroney Fail to Teach All the Independent Claim Features**

Gonzales describes a trace function that can operate in two modes. In the first mode, which is known as normal diagnostic mode, the trace function and the CPU are linked together so that the CPU is halted whenever the trace function (i.e., the FIFO) is halted. The trace function is halted in response to an event condition. A user can then examine the contents of the FIFO to determine the flow of software instructions that were executed prior to the event. In the second mode, called a FIFO halt mode, the CPU is not halted when the FIFO is halted to enable real time debug of the CPU. The second mode is used with debugging systems that require real time functionality, e.g., debugging a Hard Disk Drive controller. While the trace function is stopped to allow the debugger to access information from the FIFO, the CPU keeps on running

its application. Halting the FIFO could be viewed as "suppressing the capture of diagnostic data." Whether the FIFO is halted and the CPU continues to run depends on bits in the control register of the controller. See col. 4, lines 30 – 38 and Table IV. The FIFO may also be halted in response to an event condition. Event conditions are listed in Table II. These conditions are all linked to usual requests (breakpoints, external debug request, trace request). But none is linked to the domain in which the processor is operating. Furthermore, the capturing of diagnostic data is simply stopped in Gonzales by halting the FIFO, it is not suppressed in one domain while being allowed in another.

The combination of Gonzales and Moroney, even if it could be made for purposes of argument, fails to disclose or suggest "a processor operable in...a plurality of domains" and "control logic configured to control said monitoring logic in dependence on said at least one control parameter and the domain in which said processor is operating to suppress capturing of diagnostic data relating to predetermined activities of said processor in said first domain while allowing capturing of diagnostic data relating to predetermined activities of said processor in said second domain," as recited in claim 1.

Gonzales is not concerned with secure data, and the Examiner admits that Gonzales lacks (1) a processor that operates in two different domains and (2) a teaching "that while diagnostic data capture is being suppressed in one domain, capturing of diagnostic data in the second domain is allowed" and relies on Moroney.

Moroney tries to provide flexible security for reprogrammable devices so they are "not susceptible to later attack by pirates." Col. 1:57-59. Information can be downloaded across two different links via two inputs to the download port 116. Unfettered access for information download is available over a first link via a first fuse circuit 120-1 until that fuse is broken. Partially restricted access is available over a second link via a second fuse circuit 120-2. But

over the second link, the code ciphertext "must be decrypted by the cryptoengine 128 before it is useful." Col. 4, lines 12-14.

The Examiner maps the two paths or links onto the claimed first and second domains. But this mapping is unreasonable. The claimed processor is operable in a plurality of domains, meaning that it operates in two different domains called the first and second domains. It does not make sense to argue that a domain is a path or link because a processor does not operate in a path or link. Rather, a processor merely sends or receives data over a path or link. This interpretation problem is further highlighted by the claim recitation: the "control logic is configured to control said monitoring logic...to suppress capturing of diagnostic data relating to predetermined activities of said processor in said first domain." A processor cannot have activities in a path that downloaded data is transmitted along. In addition, a person of ordinary skill in the art would not consider a download path or link to be a processor operation domain as the term would be understood in this art and especially in light of the specification and figures, see, e.g., the non-limiting illustration in Figure 2 and related description. Thus, the Examiner's interpretation of Moroney's download paths as processor operating domains cannot be reasonably maintained.

Claim 1 also recites "a storage element configured to store at least one control parameter." The Examiner refers to col. 3, lines 29 – 32 of Gonzales for this feature. This text describes a SERIAL I/O signal that is received by the controller, but it does not disclose that the SERIAL I/O signal is stored in a storage element. Instead, the SERIAL I/O signal directs the controller to either halt the CPU and the FIFO or just halt the FIFO depending on the signals received. Thus, this section does not disclose a storage element for storing the claimed control parameter.

**Clear Error #2: Gonzales and Moroney Cannot Be Reasonably Combined**

There is no reasonable basis for combining Gonzales and Moroney. Moroney is concerned with maintaining the security of downloaded data, while Gonzales is concerned with monitoring a processor. The Examiner does not explain how Moroney's two paths for supplying downloaded data could be included in Gonzales. This is particularly problematic because neither Gonzales nor Moroney teach a processor operable in two different domains.

Even if Moroney's two paths could somehow be used to allow diagnostic data to be captured in one domain while suppressing it in another, (for which there is no teaching or suggestion in either reference), that would mean the path that supplies diagnostic data from the bus to the FIFO would have to be replaced with two paths so that diagnostic data could be sent down one of the paths at any one time, but never down both. But Gonzales stops the FIFO from collecting data in response to a FIFO halt mode so that the user can examine the sequence in the FIFO while the CPU is running. This is considered by the Examiner to be the suppressing of capture of the diagnostic data in one domain. When data capture is suppressed, there is no reason to collect data down a different path because the collection of data has been stopped in order to halt the filling of the FIFO. There is no reason articulated as to why a skilled person would want to replace the single path from the bus to the FIFO in Gonzales with two paths.

**Clear Error #3: Gonzales and Moroney Fail to Address the Same Problem as the Claims**

In contrast to Gonzales and Moroney, the claimed technology selectively stops the monitoring logic from capturing data relating to the activities of the processor when the processor is operating in a given domain. Such a domain may be for example a secure domain or any domain where it is desired to prevent processor activity from being monitored by an external

debugger. The condition to suppress the capturing of data is hence related to the domain the processor is running in, and not just to the usual debug events as in Gonzales.

The claimed technology also addresses and solves the problem of data leaking between domains during diagnostic monitoring by enabling suppression of data capture one domain while allowing it in another. Neither Gonzales nor Moroney is concerned with this data leakage problem between domains. Instead, Gonzales allows trace data to be output from a processor while the CPU is still functioning, and Moroney provides different levels of access to memory through fused paths.

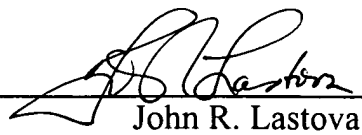
**Clear Error #4: Gonzales Fails to Teach the Features of Claims 2 and 11**

The Examiner maintains the rejection of claims 2 and 11 based on Gonzales. The Examiner equates the normal diagnostic mode (CPU and FIFO halted) in Gonzales as the claimed non-secure mode and the FIFO halt mode (FIFO halted and CPU running) in Gonzales as the claimed secure mode. But there is no indication of what the Examiner considers to be the secure domain and the non-secure domain in Gonzales. In fact, the claimed domains are not disclosed in Gonzales, as admitted by the Examiner on page 3 of the final rejection.

The Examiner is also requested to acknowledge consideration of the IDS filed on April 19, 2007 and to correct the inventor's last name ("Orion" not "Orino") in the USPTO database.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By: 

John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000